RCL circuit equations

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Summary. RCL networks are widely used for the modeling and simulation of the interconnect of today's complex VLSI circuits. In realistic simulations, the number of these RCL networks and the number of circuit elements of each of these networks is so large that model reduction has become indispensable. We describe the general class of descriptor systems that arise in the simulation of RCL networks, and mention two particular benchmark problems.

1 Motivation

Today's state-of-the-art VLSI circuits contain hundreds of millions of transistors on a single chip, together with a complex network of "wires", the so-called interconnect. In fact, many aspects of VLSI circuits, such as timing behavior, signal integrity, energy consumption, and power distribution, are increasingly dominated by the chip's interconnect. For simulation of the interconnect's effects, the standard approach is to stay within the well-established lumped-circuit paradigm [9] and model the interconnect by simple, but large subcircuits that consist of only resistors, capacitors, and inductors; see, e.g., [1, 6, 7]. However, realistic simulations require a very large number of such RCL subcircuits, and each of these subcircuits usually consists of a very large number of circuit elements. In order to handle these large subcircuits, model-order reduction methods have become standard tools in VLSI circuit simulation. In fact, many of the Krylov subspace-based reduction techniques for large-scale linear dynamical systems were developed in the context of VLSI circuit simulation; see, e.g., [2, 3, 4] and the references given there.

In this brief note, we describe the general class of descriptor systems that arise in the simulation of RCL subcircuits, and mention two particular benchmark problems.

2 Modeling

We consider general linear RCL circuits that consist of only resistors, capacitors, inductors, voltage sources, and current sources. The voltage and current sources drive the circuit, and the voltages and currents of these sources are viewed as the inputs and outputs of the circuit. Such RCL circuits are modeled as directed graphs whose edges correspond to the circuit elements and whose nodes correspond to the interconnections of the circuit elements; see, e.g., [9]. For current sources, the direction of the corresponding edge is chosen as the direction of the current flow, and for voltages sources, the direction of the corresponding edge is chosen from "+" to "-" of the source. For the resistors, capacitors, and inductors, the direction of the currents through these elements is not known beforehand, and so arbitrary directions are assigned to the edges corresponding to these elements. The directed graph is described by its *incidence matrix* $A = [\, a_{jk} \,]$. The rows and columns of A correspond to the nodes and edges of the directed graph, respectively, where $a_{jk} = 1$ if edge k leaves node j, $a_{jk} = -1$ if edge k enters node j, and $a_{jk} = 0$ otherwise.

We denote by v_n the vector of nodal voltages, i.e., the j-th entry of v_n is the voltage at node j. We denote by v_e and i_e the vectors of edge voltages and currents, respectively, i.e., the k-th entry of v_e is the voltage across the circuit element corresponding to edge k, and the k-th entry of i_e is the current through the circuit element corresponding to edge k. Finally, we use subscripts r, c, l, v, and i to denote edge quantities that correspond to resistors, capacitors, inductors, voltage sources, and current sources of the RCL circuit, respectively, and we assume that the edges are ordered such that we have the following partitionings:

$$A = [\, A_r \quad A_c \quad A_l \quad A_v \quad A_i \,], \quad v_e = \begin{bmatrix} v_r \\ v_c \\ v_l \\ v_v \\ v_i \end{bmatrix}, \quad i_e = \begin{bmatrix} i_r \\ i_c \\ i_l \\ i_v \\ i_i \end{bmatrix}. \tag{1}$$

The RCL circuit is described completely by three types of equations: *Kirchhoff's current laws* (KCLs), *Kirchhoff's voltage laws* (KVLs), and the *branch constitutive relations* (BCRs); see, e.g., [9]. Using the partitionings (1), these equations can be written compactly as follows. The KCLs state that

$$A_r i_r + A_c i_c + A_l i_l + A_v i_v + A_i i_i = 0, \tag{2}$$

the KVLs state that

$$A_r^T v_n = v_r, \quad A_c^T v_n = v_c, \quad A_l^T v_n = v_l, \quad A_v^T v_n = v_v, \quad A_i^T v_n = v_i, \tag{3}$$

and the BCRs state that

$$i_r = R^{-1} v_r, \quad i_c = C \frac{d}{dt} v_c, \quad v_l = L \frac{d}{dt} i_l. \tag{4}$$

Here, R and C are positive definite diagonal matrices whose diagonal entries are the resistances and capacitances of the resistors and capacitors, respectively. The diagonal entries of the symmetric positive definite matrix L are the inductances of the inductors. Often L is also diagonal, but in general, when mutual inductances are included, L is not diagonal. In (2)–(4), the known vectors are the time-dependent functions $v_v = v_v(t)$ and $i_i = i_i(t)$ the entries of which are the voltages and currents of the voltage and current sources, respectively. All other vectors are unknown time-dependent functions.

3 Formulation as first-order descriptor systems

The circuit equations (2)–(4) can be rewritten in a number of different ways. For example, for the special case of RCL circuits driven only by voltage sources, a formulation as systems of first-order integro-DAEs is given in [5].

Here, we present a formulation of (2)–(4) as a structured descriptor system. Recall that the currents $i_i(t)$ of the current sources, and the voltages $v_v(t)$ of the voltage sources are known functions of time. In the setting of a descriptor system, these quantities are the entries of the system's input vector $u(t)$ as follows:

$$u(t) = \begin{bmatrix} -i_i(t) \\ v_v(t) \end{bmatrix}. \tag{5}$$

The voltages $v_i(t)$ across the current sources, and the currents $i_v(t)$ through the voltage sources, are unknown functions of time, and these quantities are the entries of the system's output vector $y(t)$ as follows:

$$y(t) = \begin{bmatrix} v_i(t) \\ -i_v(t) \end{bmatrix}. \tag{6}$$

Note that we can use the first three equations in (3) and the BCRs (4) to readily eliminate the parts v_r, v_c, v_l of the edge voltages and the parts i_r, i_c of the edge currents. Therefore, in addition to the input and output variables (5) and (6), only the nodal voltages v_n and the inductor currents i_l remain as unknowns, and we define the system's state vector $x(t)$ as follows:

$$x(t) = \begin{bmatrix} v_n(t) \\ i_l(t) \\ i_v(t) \end{bmatrix}. \tag{7}$$

Performing the above eliminations of v_r, v_c, v_l, i_r, i_c and using (5)–(7), one easily verifies that the RCL circuit equations (2)–(4) are equivalent to the descriptor system,

$$\begin{aligned} \mathcal{E}\,\frac{d}{dt}x(t) &= \mathcal{A}\,x(t) + \mathcal{B}\,u(t), \\ y(t) &= \mathcal{B}^T x(t), \end{aligned} \tag{8}$$

where

$$\mathcal{A} := -\begin{bmatrix} A_r R^{-1} A_r^T & A_l & A_v \\ -A_l^T & 0 & 0 \\ -A_v^T & 0 & 0 \end{bmatrix}, \quad \mathcal{E} := \begin{bmatrix} A_c C A_c^T & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & 0 \end{bmatrix}, \tag{9}$$

$$\mathcal{B} := \begin{bmatrix} A_i & 0 \\ 0 & 0 \\ 0 & -I \end{bmatrix},$$

and I denotes the identity matrix. Moreover, the block sizes in (9) correspond to the partitionings of the input, output, and state vectors in (5)–(7).

4 Two particular benchmark problems

The first benchmark problem, called the *PEEC problem*, is a circuit resulting from the so-called PEEC discretization [8] of an electromagnetic problem. The circuit is an RCL circuit consisting of 2100 capacitors, 172 inductors, 6990 inductive couplings, and a resistive source that drives the circuit.

Table 1. System matrices for the PEEC problem.

matrix	m	n	nnz	Is symmetric?
$\mathcal{A}$	306	306	696	no
$\mathcal{E}$	306	306	18290	yes
$\mathcal{B}$	306	2	2	no

The second example, called the *package problem*, is a 64-pin package model used for an RF integrated circuit. Only eight of the package pins carry signals, the rest being either unused or carrying supply voltages. The package is characterized as a 16-port component (8 exterior and 8 interior terminals). The package model is described by approximately 4000 circuit elements, resistors, capacitors, inductors, and inductive couplings.

Table 2. System matrices for the package problem.

matrix	m	n	nnz	Is symmetric?
$\mathcal{A}$	1841	1841	5881	no
$\mathcal{E}$	1841	1841	5196	yes
$\mathcal{B}$	1841	16	24	no

5 Acknowledgment

The author is indebted to Peter Feldmann for first introducing him to VLSI circuit simulation, and also for providing the two benchmark problems mentioned in this paper.

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